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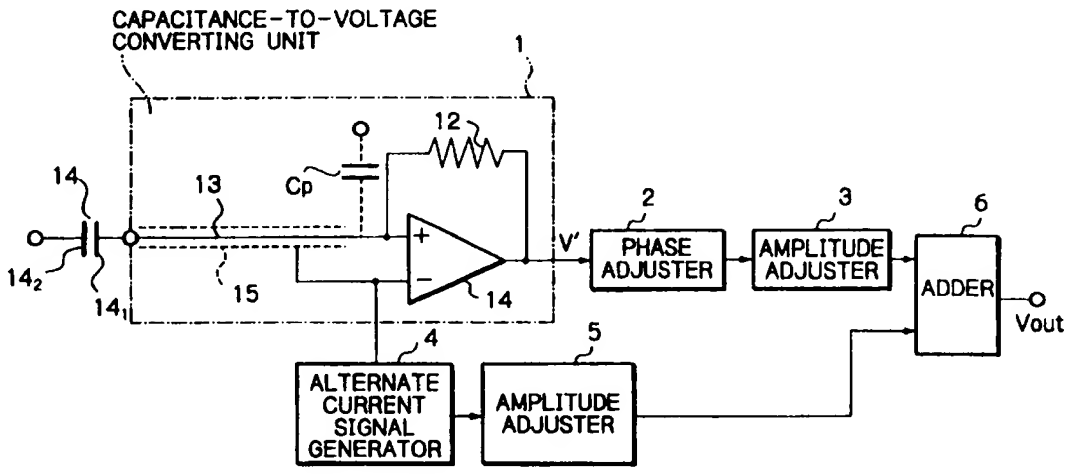

(57) Abstract

A static capacitance–to–voltage converter is capable of converting a static capacitance into a voltage without suffering from a stray capacitance formed between a signal and a shielding line or a stray capacitance formed between an exposed portion of the signal line and its surroundings. The static capacitance–to–voltage converter is formed of an operational amplifier placed in an imaginary short–circuit state between an inverting input and a non–inverting input thereof; a signal line having one end connected to the inverting input and the other end capable of being connected to a static capacitance; a shielding line surrounding the signal line and connected to the non–inverting input; an alternate current signal generator for applying the non–inverting input with an alternate current signal; and zero adjusters for adjusting the output of the static capacitance–to–voltage converter to minimum when no static capacitance is connected to the signal line.

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DESCRIPTION

STATIC CAPACITANCE-TO-VOLTAGE CONVERTER AND CONVERTING METHOD

TECHNICAL FIELD

The present invention relates to a static capacitance-to-voltage converter and an associated converting method which are capable of highly accurate convertsion of a static capacitance into a corresponding voltage by eliminating the influence of a stray capacitance occurring on a signal line for connecting the static capacitance to an operational amplifier.

BACKGROUND ART

Fig. 1 generally illustrates the configuration of a static capacitance-to-voltage converter described in Laid-open Japanese Patent Application No. 61-14578. This static capacitance-to-voltage converter has been proposed to solve a problem of the prior art which suffers from the inability of accurate voltage conversion due to the fact that a stray capacitance of a cable used to connect an unknown static capacitance is superimposed on the unknown static capacitance, and that these static capacitances may vary due to movements and bending of the cable or the like. As illustrated in Fig. 1, an unknown capacitance Cx is connected between an alternate current (AC) signal generator OS and an operational amplifier OP with connection cables covered with shielding lines S to reduce the influence of stray capacitances Cs1, Cs2, Cs3. Specifically, an output and an inverting input of the operational amplifier OP are

connected through a feedback circuit formed of a parallel circuit including a resistor Rf and a capacitor Cf. The unknown capacitance Cx has one end connected to the inverting terminal of the operational amplifier OP through a shielding line s, and the other end connected to the AC signal generator OS through another shielding line s. Both of the shielding lines and a non-inverting input of the operational amplifier OP are grounded.

With the configuration described above, since substantially no voltage difference exists between the two ends of the unknown capacitance Cx, the stray capacitance Cs2 is not charged. Also, since the stray capacitance Cs3 is regarded as a coupling capacitance of both the shielding lines s, the stray capacitance Cs3 can be eliminated by grounding the shielding lines s. In this way, the influence exerted by the stray capacitances of the cables for connecting the unknown capacitance Cx is reduced by using the shielding lines s, so that a charge equal to that induced on the unknown static capacitance Cx is induced on the capacitor Cf of the feedback circuit, resulting in an output proportional to the unknown static capacitance Cx produced from the operational amplifier OP. Stated another way, assuming that an output voltage of the AC signal generator OS is Vi, an output voltage Vo of the operational amplifier OP is expressed by $-(Cx/Cf)Vi$, so that the converter of Fig. 1 may be used to convert the unknown static capacitance Cx into the voltage Vo from which the unknown static capacitance Cx can be derived together with

the known values Cf and Vi.

SUMMARY OF THE INVENTION

The static capacitance-to-voltage converter illustrated in Fig. 1, however, implies a problem that as the unknown static capacitance Cx is smaller, the influence of stray capacitances becomes prominent, so that the static capacitance Cx cannot be accurately converted into a voltage. In addition, since the feedback circuit of the operational amplifier OP is formed of a parallel circuit including the resistor Rf and the capacitor Cf, separate steps are required to form a resistor and a capacitor for actually integrating necessary components into a converter in a one-chip form, causing disadvantages of a complicated manufacturing process and an increased chip size. Furthermore, since the capacitor cannot be applied with an AC signal when one electrode of the static capacitance Cx is being biased at a certain voltage, a conversion of the static capacitance into an output voltage cannot be performed.

To solve the problem as mentioned, the applicant has proposed a static capacitance-to-voltage converter constructed as illustrated in Fig. 2. In the following, this static capacitance-to-voltage converter will be described in detail with reference to Fig. 2. An operational amplifier 21 has a voltage gain extremely larger than a closed loop gain. A gain seems to be almost infinity. A feedback resistor 23 is connected between an output terminal 22 and an inverting input terminal (-) of the operational amplifier 21 to form a negative feedback for

the operational amplifier 21. The operational amplifier 21 has a non-inverting input terminal (+) connected to an alternate current (AC) signal generator 24 and the inverting input terminal (-) connected to one end of a signal line 25 which has the other end connected to one electrode 26_1 of a capacitor 26 having an unknown or known static capacitance. The other electrode 26_2 of the capacitance 26 is grounded, clamped to a fixed direct current (DC) bias voltage or not grounded. The other electrode 26_2 may be applied with an AC bias. In this case, the bias current may have a frequency identical to or different from the frequency of an AC signal output from the AC signal generator 24.

The signal line 25 is surrounded by a shielding line 27 for preventing unwanted signals such as noise from being induced into the signal line 25 from the outside. The shielding line 27 is not grounded but is connected to the non-inverting input terminal (+) of the operational amplifier 21.

Since the operational amplifier 21 is formed with a negative feedback through the feedback resistor 23, and the operational amplifier 21 has a voltage gain extremely larger than a closed loop gain, the operational amplifier 21 is in an imaginary short-circuit state, and a gain seems to be almost infinity. In other words, an electric potential difference between the inverting input terminal (-) and the non-inverting input terminal (+) of the operational amplifier 21 is substantially zero. Thus, since the signal line 25 and the shielding line 27 are at the same voltage,

it is possible to cancel a stray capacitance possibly occurring between the signal line 25 and the shielding line 27. This holds true irrespective of the length of the signal line 25, and also holds true irrespective of movements, bending, folding and so on of the signal line 25.

Assume now that an AC output voltage of the AC signal generator 24 is Vi; its angular frequency is ω; the static capacitance of the capacitor 26 is Cx; a current flowing through the capacitance 26 is i_1; the resistance of the feedback resistor 23 is Rf; a current flowing through the feedback resistor 23 is i_2; a voltage at the inverting input terminal of the operational amplifier 21 is Vm; an output voltage of the operational amplifier 21 is V, the voltage Vm at the inverting input terminal (-) is at the same voltage as the AC signal output voltage Vi of the AC signal generator 24 since the operational amplifier 21 is in an imaginary short-circuit state, as mentioned above. That is, the following equation is satisfied:

$$Vi = Vm$$

In addition, the following equations are also satisfied:

$$i_1 = -Vm/(1/j\omega Cx) = -Vi/(1/j\omega Cx)$$

$$i_2 = (Vm-V)/Rf = (Vi=V)/Rf$$

Here, since $i_1=i_2$, the output voltage V of the operational amplifier 21 is expressed by the following equation:

$$V = Vi(1+j\omega Rf \cdot Cx)$$

This equation indicates that the output voltage V of the operational amplifier 21 includes an AC component

proportional to the static capacitance Cx. It is therefore possible to derive a DC voltage proportional to the static capacitance Cx by appropriately processing the output voltage V.

As described above, since the operational amplifier 21 is in an imaginary short-circuit state so that a stray capacitance occurring between the signal line 25 and the shielding line 27 will not appear between the inverting input terminal (-) and the non-inverting input terminal (+) of the operational amplifier 21, the equation representing the output voltage V of the operational amplifier 21 does not include a term related to the stray capacitance occurring between the signal line 25 and the shielding line 27. For this reason, a very small static capacitance Cx can be converted into a voltage. In addition, even if the AC output voltage Vi has a low angular frequency ω, a voltage V exactly corresponding to the static capacitance Cx can be output.

In the static capacitance-to-voltage converter of Fig. 2, since the signal line 25 and one end of the feedback resistor 23 are connected to the inverting input terminal (-) of the operational amplifier 21, the signal line 25 inevitably includes a portion left exposed, without being surrounded by the shielding line 27, near the end connected to the inverting input terminal. Since a stray capacitance is formed between the exposed portion of the signal line 25 and its surroundings, the influence of this stray capacitance becomes sometimes more prominent as the static

capacitance Cx is smaller, causing a problem that an accurate detection of the static capacitance Cx is prevented.

The present invention has been proposed to solve the problems mentioned above, and it is therefore an object of the present invention to provide an impedance-to-voltage converter and an associated converting method which are capable of highly accurate conversion of an impedance of an object under measurement into a corresponding voltage by utilizing an operational amplifier in an imaginary short-circuit state to eliminate the influence of a stray capacitance between a line connected to a non-inverting terminal of the operational amplifier and a shielding line surrounding the line, and eliminating the influence of a stray capacitance formed by an unshielded portion of the signal line.

To achieve the above object, the present invention provides a static capacitance-to-voltage converter comprising:

an operational amplifier having an inverting input terminal, a non-inverting input terminal and an output terminal, wherein the operational amplifier has the output terminal and the inverting input terminal connected through a feedback resistor, and operable in an imaginary short-circuit state between the inverting input terminal and the non-inverting input terminal;

a signal line having one end connected to the inverting input terminal and the other end capable of being connected to a static capacitance element having a static

capacitance;

a shield surrounding at least a portion of the signal line, and connected to the non-inverting input terminal;

alternate current signal generator for applying the non-inverting input terminal with an alternate current signal; and

an adjuster connected to the output terminal of the operational amplifier and an output terminal of the alternate current signal generator for adjusting an output of the static capacitance-to-voltage converter to minimum (almost equal to zero) when no static capacitance element is connected to the signal line.

The adjuster comprises a variable frequency generator of the alternate current signal and an adjuster for adjusting amplitudes and phases of an output signal of the operational amplifier and the alternate current signal such that they are canceled with each other.

The adjuster preferably comprises:

first adjuster for adjusting the amplitude of the alternate current signal;

second adjuster for adjusting the phase and amplitude of an output voltage from the operational amplifier such the output voltage has the same amplitude as and an opposite phase to an output of the first adjuster; and

an adder for adding the output of the first adjuster and an output of the second adjuster.

Alternatively, the adjuster preferably comprises:

third adjuster for adjusting the amplitude of the

output voltage of the operational amplifier;

fourth adjuster for adjusting the phase and amplitude of the alternate current signal such that the alternate current signal has the same amplitude as and an opposite phase to an output of the third adjuster; and

an adder for adding the output of the third adjuster and an output of the fourth adjuster.

Further, an integrator may be additionally provided for integrating an output of the adjuster, so that when a static capacitance is connected to the other end of the signal line, a signal corresponding to the static capacitance of the static capacitance can be produced as an output of the integrator. Furthermore, a comparator may be provided for comparing the phase of the output of the integrator with the phase of the alternate current signal. In this case, when a static capacitance is connected to the other end of the signal line, a signal representative of dielectric loss tangent for the static capacitance of the static capacitance can be produced as an output of the comparator.

First and second synchronous detectors may further be provided for receiving the output of the integrator and the alternate current signal, such that the first synchronous detector outputs a signal representative of the static capacitance of the static capacitance, and the second synchronous detector outputs a signal representative of dielectric loss tangent for the static capacitance of the static capacitance.

The present invention also provides a method of converting a static capacitance into a voltage comprising:

creating an imaginary short-circuit state between an inverting input terminal and a non-inverting input terminal of an operational amplifier;

connecting one end of a signal line to the inverting input terminal, where the signal line has at least a portion thereof surrounded by a shield;

placing the shield at the same voltage as the non-inverting input terminal;

applying an alternate current signal to the non-inverting input terminal;

adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line; and

connecting a static capacitance to the other end of the signal line, after the adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line, to retrieve a voltage signal corresponding to the static capacitance of the static capacitance.

Preferably, the adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are

canceled with each other when no static capacitance is connected to the other end of the signal line comprises:

varying the frequency of the alternate current signal; and

adjusting the output signal of the operational amplifier and the alternate current signal in phase and amplitude such that the output signal and the alternate current signal are canceled with each other.

Also, the adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line may comprise:

adjusting the amplitude of the alternate current signal;

adjusting the phase and amplitude of an output voltage from the operational amplifier such the output voltage has the same amplitude as and an opposite phase to the alternate current signal having its amplitude adjusted; and

adding the alternate current signal having its amplitude adjusted, and the output voltage of the operational amplifier having its phase and amplitude adjusted.

Alternatively, the adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line may comprise:

adjusting the amplitude of the output voltage of the operational amplifier;

adjusting the phase and amplitude of the alternate current signal such that the alternate current signal has the same amplitude as and an opposite phase to the output voltage of the operational amplifier having its amplitude adjusted; and

adding the output voltage having its amplitude adjusted and the alternate current signal having its phase and amplitude adjusted.

This converting method may also comprise:

integrating the voltage signal to output a signal corresponding to the static capacitance, and/or comparing the phase of the integrated signal with the phase of the alternate current signal to output a signal representative of dielectric loss tangent for the static capacitance.

Furthermore, the integrated signal may be synchronously detected with the alternate current signal to output a signal representative of the static capacitance of the static capacitance element and a signal indicative of dielectric loss tangent for the static capacitance of the static capacitance element.

The shield is preferably a shielding line surrounding the signal line over its entire length. Also, the static capacitance may be a capacitive sensor. In addition, the static capacitance may comprise a measuring electrode so that a static capacitance is formed between an object under measurement and the measuring electrode.

Furthermore, during measurement waiting time, the measuring electrode may be accommodated in a case which is placed at the same voltage as a non-inverting input terminal of the operational amplifier, and a zero adjustment is performed to cancel a stray capacitance formed between the measuring electrode and its surroundings.

Since the operational amplifier is placed in an imaginary short-circuit state between the inverting input terminal and the non-inverting input terminal, a stray capacitance formed between the signal line and the shielding line is canceled. Also, by adjusting the static capacitance-to-voltage converter so that its output is minimum (almost equal to zero) when no static capacitance is connected to the signal line, the static capacitance-to-voltage converter is free from the influence of a stray capacitance formed by an exposed portion of the signal line. Thus, a voltage corresponding to a static capacitance is output without suffering from such stray capacitances, however long the signal line and the shield are.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit diagram illustrating an example of a prior art static capacitance-to-voltage converter;

Fig. 2 is a schematic circuit diagram illustrating a static capacitance-to-voltage converter proposed by the applicant for solving drawbacks of the static capacitance-to-voltage converter of Fig. 1;

Fig. 3 is a block diagram generally illustrating the

configuration of a first embodiment of a static capacitance-to-voltage converter according to the present invention;

Fig. 4 is a circuit diagram illustrating an example of a specific configuration of the static capacitance-to-voltage converter of Fig. 3;

Fig. 5 is a block diagram illustrating the configuration of a capacitance meter which applies the static capacitance-to-voltage converter shown in Fig. 3;

Fig. 6 is a block diagram illustrating an example of a modification to the capacitance meter shown in Fig. 5;

Fig. 7 is a block diagram generally illustrating the configuration of a second embodiment of the static capacitance-to-voltage converter according to the present invention;

Fig. 8 is a circuit diagram illustrating an example of a specific configuration of the static capacitance-to-voltage converter of Fig. 7;

Fig. 9 is a block diagram illustrating the configuration of a capacitance meter which applies the static capacitance-to-voltage converter shown in Fig. 7; and

Fig. 10 is a block diagram illustrating an example of a modification to the capacitance meter shown in Fig. 9.

Fig. 11 shows an experimental result obtained from the example of a static cpacitance-to-voltage converter shown in Fig. 4. In this example, suitable electric components are chosen in the electric circuits.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention will hereinafter be described in

detail in connection with preferred embodiments thereof with reference to the accompanying drawings. Fig. 3 is a block diagram generally illustrating a first embodiment of a static capacitance-to-voltage converter according to the present invention. Referring specifically to Fig. 3, the static capacitance-to-voltage converter comprises a capacitance-to-voltage converting unit 1; a phase adjuster 2 for adjusting the phase of an output voltage of the capacitance-to-voltage converting unit 1; a first amplitude adjuster 3 for adjusting the amplitude of a phase adjusted voltage; an alternate current (AC) signal generator 4 having a variable frequency generator; a second amplitude adjuster 5 for adjusting the amplitude of an AC signal from the AC signal generator 4; and an adder 6 for adding voltages output from the first amplitude adjuster 3 and the second amplitude adjuster 4.

The capacitance-to-voltage converting unit 1 includes an operational amplifier 11 which may be an amplifier having a voltage gain extremely larger than a closed loop gain. A gain seems to be almost infinity. A feedback resistor 12 is connected between an output and an inverting input terminal (-) of the operational amplifier 11 to form a negative feedback for the operational amplifier 11. The operational amplifier 11 has a non-inverting input terminal (+) applied with an AC signal from the AC signal generator 4, and the inverting input terminal (-) connected to one end of a signal line 13. The other end of the signal line 13 may be connected to a static capacitance element 14 having a static

capacitance Cx such as a capacitor or the like. The static capacitance element 14 includes one electrode 14_1 and the other electrode 14_2 which is grounded, clamped to a fixed DC bias voltage, or not grounded. Alternatively, the other electrode 14_2 may be applied with an AC bias having a frequency identical to or different from the frequency of the AC signal from the AC signal generator 4. While an ambient AC signal is further applied to the inverting input terminal (-) through a stray capacitance Cp, this AC signal generally has a frequency which is different from that of the AC signal from the AC signal generator 4 and that of the AC bias applied to the electrode 14_2.

The signal line 13 is surrounded by a shielding line 15 for preventing unwanted signals such as noise from being induced into the signal line 13 from the outside. The shielding line 15 is not grounded but is connected to the non-inverting input terminal (+) of the operational amplifier 11.

The capacitance-to-voltage converting unit 1 has substantially the same configuration as a static capacitance-to-voltage converter illustrated in Fig. 7. Specifically, since the operational amplifier 11 is formed with a negative feedback through the feedback resistor 12, the operational amplifier 11 has a voltage gain extremely larger than a closed loop gain, and a gain seem to be almost infinity, the operational amplifier 11 is in an imaginary short-circuit state between both the input terminals thereof. In other words, a difference in voltage between the

inverting input terminal (-) and the non-inverting input terminal (+) of the operational amplifier 11 is substantially zero. Thus, since the signal line 13 and the shielding line 15 are at the same electric potential (so-called voltage), it is possible to cancel a stray capacitance possibly occurring between the signal line 13 and the shielding line 15. This holds true irrespective of the length of the signal line 13, and also holds true irrespective of movements, bending, folding and so on of the signal line 13.

However, since the signal line 13 has a portion near the end connected to the inverting input terminal (-) of the operational amplifier 11 left exposed, without being shielded by the shielding line 15, a stray capacitance Cp is formed between the exposed portion of the signal line 13 and its surroundings. This stray capacitance Cp adversely affects the output voltage of the operational amplifier 11 and hence an output voltage V' of the capacitance-to-voltage converting unit 1, with the result that the output voltage V' fails to accurately represent the static capacitance of the static capacitance element 14.

To eliminate the influence of the stray capacitance Cp, in the first embodiment of the present invention, the frequency of the AC signal output from the AC signal generator 4 is adjusted to reduce the output voltage Vout of the adder 6 to substantially zero when the static capacitance element 14 is not connected to the other end of the signal line 13, as well as the phase and amplitude of

the output voltage V' is adjusted by the phase adjuster 2 and the first amplitude adjuster 3, respectively, and the amplitude of the AC signal from the AC signal generator 4 is adjusted by the second amplitude adjuster 5 such that the output of the first amplitude adjuster 3 has the same amplitude as and the opposite phase to the output of the second amplitude adjuster 5. Then, the two outputs are added by the adder 6. In this way, the outputs of the first amplitude adjuster 3 and the second amplitude adjuster 5 are canceled.

Stated another way, a variable frequency generator of the AC signal generator 4, the phase adjuster 2, the first amplitude adjuster 3, the second amplitude adjuster 5, and the adder 6 constitute an adjuster which minimizes electric potential difference or which adjusts electric potential difference. When the static capacitance element 14 is connected to the other end of the signal line 13 after minimizing or a zero adjustment has been made, a voltage Vout exactly corresponding to the static capacitance of the static capacitance element 14 is output from the adder 6 without suffering from the influence of the stray capacitance Cp and a stray capacitance between the signal line 13 and the shielding line 15.

Fig. 4 is a circuit diagram illustrating an example of the configuration and interconnections between various components of the static capacitance-to-voltage converter of Fig. 3. Fig. 4 shows resistors R1 - R13; a capacitor C1; operational amplifiers AMP1 - AMP6; an AC signal Vin having

an angular frequency ω; and a bias voltage Vs which is applied to non-inverting input terminals of respective operational amplifiers in the phase adjuster 2, the first amplitude adjuster 3, the second amplitude adjuster 5 and the adder 6. It should be noted that the capacitance-to-voltage converting unit 1 in Fig. 4 is composed of the resistor R1 representative of the feedback resistor 12 and the operational amplifier AMP1 representative of the operational amplifier 11. The AC signal generator 4 in turn is configured to apply the output Vin of an oscillator to a buffer including the operational amplifier AMP4 to produce an output voltage Vd (=Vin).

In the following, the operation of the static capacitance-to-voltage converter in Fig. 4 will be described from a mathematical viewpoint. Assume now that the output voltage of the capacitance-to-voltage converting unit 1 is Va; the output voltage of the phase adjuster 2 is Vb; the output voltage of the first amplitude adjuster 3 is Vc; the output voltage of the AC signal generator 4 is Vd; the output voltage of the second amplitude adjuster 5 is Ve; and R3=R4. Further, assuming Vs=0 for simplifying the calculation, the following equation is satisfied:

$$Va = Vin[1+R1 \cdot j\omega(Cx+Cp)]$$

$$Vb = Va(1-R5 \cdot j\omega C1)/(1+r5 \cdot j\omega C1)$$

$$Vc = (R7/R6)Vb$$

$$Vd = Vin$$

$$Ve = (R11/R10)Vin$$

$$Vout = -(R9/R8)Vc+[1+(R9/R8)]x[R13/(R12+R13)]Ve$$

Therefore, the output voltage Vout of the adder 6 is expressed by the following equation:

$$Vout = (R9/R8)(R7/R6) \times \{[1+R1 \cdot j\omega(Cx+Cp)](1-R5 \cdot j\omega C1) / (1+R5 j\omega C1)\}Vin - \{1+(R9/R8)[R13/(R12+R13)]\} \times (R11/R10)Vin$$

Here, when the resistances are selected such that R1=R2, R6=R7, R8=R9, R10=2R11, R12=R13 are satisfied, the output voltage Vout of the adder 6 can be rewritten as follows:

$$Vout = \{[1+R1 \cdot j\omega(Cx+Cp)](1-R5 \cdot j\omega C1)/(1+R5 \cdot j\omega C1)\}Vin-2Vin \quad (1)$$

In the present invention, first, when the static capacitance element 14 is not connected to the signal line 13, i.e., when Cx=0, the phase and amplitude of the output voltage of the capacitance-to-voltage converting unit 1 and the angular frequency and amplitude of the AC signal output from the AC signal generator 4 are adjusted such that Vout in the equation (1) is zero. Substituting Vout=0 in the equation (1) for finding a condition in which Vout is zero, the following equation is derived:

$$\{[1+R1 \cdot j\omega(Cp)](1-R5 \cdot j\omega C1)/(1+R5 \cdot j\omega C1\}-2 = 0$$

This equation is rewritten in the following form:

$$R1R5\omega^2C1Cp-1+(R1Cp-3R5C1)j\omega = 0$$

To satisfy this equation, the following conditions must be met:

$$R1R5\omega^2C1Cp = 1 \quad (2)$$

$$R1Cp = 3R5C1 \quad (3)$$

Thus, substituting the equation (3) into the equation (2), and solving the equation (2) for ω,

$$\omega = 1/(R1CpR5C1)^{1/2}$$

$$= 1/[(3)^{1/2}R5C1] \quad (4)$$

is derived.

As will be understood from the foregoing, in the present invention, R5, C1 and ω are adjusted so as to satisfy the equations (3) and (4) in a state in which the static capacitance element 14 is not connected to the signal 13, so that the output voltage Vout of the adder 6 becomes zero.

Next, when the static capacitance element 14 is connected to the signal line 13, the following equation is satisfied as mentioned above:

$$\{[1+R1\cdot j\omega(Cp)](1-R5\cdot j\omega C1)/$$

$$(1+R5\cdot j\omega C1\}Vin-2Vin = 0$$

Further, since the equations (3) and (4) are satisfied, the equation (1) can be rewritten as follows:

$$Vout = R1\cdot j\omega Cx(1-R5\cdot j\omega C1)$$

$$/(1+R5\cdot jC1)$$

Substituting this into the equation (4), Vout is expressed as follows:

$$Vout = (4/3)VinR1\cdot j\omega Cx \quad (5)$$

This equation (5) indicates that the output voltage Vout of the adder 6 is not influenced at all by any static capacitance other than the static capacitance Cx of the static capacitance element 14.

As described above in detail, since the static capacitance-to-voltage converter illustrated in Figs. 3 and 4 cancels a stray capacitance formed between the signal line 13 and the shielding line 15, and a stray capacitance formed between the exposed portion of the signal line 13 and its surroundings, it can output a voltage exactly corresponding to the static capacitance Cx of the static capacitance element 14 without suffering from the influence of such stray capacitances.

In the description heretofore made, connecting the static capacitance element 14 having the static capacitance Cx to the signal line 13 is equivalent to a change in the static capacitance connected to the inverting input terminal of the operational amplifier AMP1 by Cx. Therefore, the static capacitance-to-voltage converter of Figs. 3 and 4 can also output a voltage exactly corresponding to ΔCx when the static capacitance Cx of the static capacitance element 14 connected to the signal line 13 has changed by ΔCx. In the following, this operation will be described in detail in connection with the static capacitance-to-voltage converter of Fig. 4.

The output voltage Vout of the adder 6 when the static capacitance element 14 is connected to the signal line 13 is expressed by the aforementioned equation (1). Assume that Vout is zero in this condition. Conditions for satisfying this can be found by giving Vout=0 in the equation (1):

$$R5C1 = (1/3)R1(Cx+Cp) \quad (6)$$

$$\omega = 1/(3)^{1/2} R5C1 \quad (7)$$

Stated another way, the output voltage Vout of the adder 6 can be made zero by adjusting the angular frequency ω of the AC signal from the AC signal generator 4, R5 and C1 to satisfy the equations (6) and (7).

Next, the output voltage Vout of the adder 6, when the static capacitance Cx of the static capacitance element 14 has changed by ΔCx, can be expressed by substituting $Cx+\Delta Cx$ for Cx in the equation (1):

$$Vout = \{[1+R1 \cdot j\omega(Cx+\Delta Cx+Cp)] \times (1-R5 \cdot j\omega C1)/(1+R5 \cdot j\omega C1)\}Vin - 2Vin \quad (8)$$

Then, substituting the equations (6) and (7) into the equation (8), and using V=0 in the equation (1):

$$Vout = (4/3)VinR1 \cdot j\omega\Delta Cx \quad (9)$$

This equation indicates that Vout exactly corresponds to ΔCx. This also indicates that the static capacitance-to-voltage converter of Fig. 4 is capable of outputting a voltage exactly corresponding to a change in capacitance of the static capacitance element 14 connected to the signal line 13.

While the foregoing description has been made on the assumption that Vs=0 is satisfied, the same conclusion is derived also when $Vs \neq 0$, only except that associated calculations are more complicated. Alternatively, in Figs. 3 and 4, a subtractor may be used in place of the adder 6 such that the subtractor is applied with the output of the first amplitude adjuster 3 and the output of the second amplitude adjuster 5 which are adjusted to have the same

amplitude and the same phase.

Next, a capacitance meter, which is an exemplary application of the static capacitance-to-voltage converter illustrated in Fig. 3, will be described with reference to Fig. 5. This capacitance meter is configured such that an integrator 16 is connected additionally to the adder in Fig. 3, and outputs of the integrator 16 and the AC signal generator 4 are connected to a phase comparator 17.

As mentioned above, the output voltage Vout of the adder 6 is expressed by the equations (5) and (9). By integrating this voltage by the integrator 16, it is possible to produce a voltage E which is proportional to the static capacitance Cx of the static capacitance element 14 or a change ΔCx in the static capacitance Cx. Also, by using the phase comparator 17 to derive a difference in phase between the voltage E output from the integrator 16 and the AC signal Vin output from the AC signal generator 4, dielectric loss tangent can be derived for the static capacitance element 14.

In a manner similar to the foregoing, the capacitance meter illustrated in Fig. 5 may also be designed such that one electrode 14_1 of the static capacitance element 14 is used as a measuring electrode, and the other electrode 14_2 is used as an object under measurement for which a determination is made as to whether it is good or bad based on the magnitude of a static capacitance Cx formed between the one electrode 14_1 and the other electrode 14_2. In this case, a housing for the capacitance meter is provided with a

case having the same electric potential (so-called voltage) as the operational amplifier 11. After the measuring electrode is accommodated in this case, the output voltage Vout of the adder 6 is adjusted to a minimum or zero. In this event, if the measuring electrode is taken out of the case during a measurement, the adder 6 experiences a drift by a voltage proportional to a stray capacitance between the measuring electrode and its surroundings. Therefore, a static capacitance between the measuring electrode and the object under measurement can be more accurately measured by correcting the phase adjuster 2, the first amplitude adjuster 3 and the second amplitude adjuster 5 such that the drift value becomes minimum or zero. When a measurement was actually made using a semiconductor device made of silicon, the capacitor meter was able to measure a very small static capacitance on the order of 1 femtofarad to 2 femtofarad, thereby demonstrating that the present invention is significantly effective.

Fig. 6 is a block diagram generally illustrating an exemplary modification to the capacitor meter illustrated in Fig. 5, where the output of the integrator 16 in Fig. 5 is connected to a first synchronous detector 18 and a second synchronous detector 19, such that these synchronous detectors 18, 19 are applied with an AC signal from an AC signal generator 4. When the first synchronous detector 18 synchronously detects a voltage E output from the integrator 16 with the AC signal Vin which is in phase with the voltage E, the static capacitance Cx of a static capacitance element

14 or a change ΔCx in the static capacitance Cx can be derived as an output of the first synchronous detector 18. Similarly, when the second synchronous detector 19 synchronously detects the voltage E from the integrator 16 with the AC signal Vin which is out of phase by 90° from the voltage E, dielectric loss tangent for the static capacitance element 14 can be derived as an output of the second synchronous detector 19.

More specifically, the static capacitance Cx of the static capacitance element 14 can be derived by the first synchronous detector 18 as an average value or an integrated value of the voltage E over a range from 0° to 180° with respect to the phase of the AC signal Vin from the AC signal generator 4. Also, the dielectric loss tangent for the static capacitance Cx of the static capacitance element 14 can be derived by the second synchronous detector 19 as an average value or an integrated value of the voltage E over a range from 90° to 270° with respect to the phase of the AC signal Vin from the AC signal generator 14.

Next, a second embodiment of the static capacitance-to-voltage converter according to the present invention will be described with respect to the configuration with reference to Fig. 7. The second embodiment illustrated in Fig. 7 differs from the first embodiment illustrated in Fig. 3 in that the phase adjuster 2 is not connected between the capacitance-to-voltage converting unit 1 and the first amplitude adjuster 3, but between the AC voltage generator 4 and the second amplitude adjuster 5. While in the layout

illustrated in Figs. 3 and 4, high harmonic components of the AC signal Vin output from the AC signal generator 4 may be introduced into the phase adjuster 2 or the first amplitude adjuster 3, such an inconvenience can be effectively prevented by connecting the phase adjuster 2 between the AC signal generator 4 and the second amplitude adjuster 5, as illustrated in Fig. 7.

Fig. 8 is a circuit diagram illustrating an example of the configuration of each component in the static capacitance-to-voltage converter of Fig. 7 and interconnections between these components, wherein components identical or similar to those illustrated in Fig. 4 are designated the same reference numerals. Note, however, that the configuration of the first amplitude adjuster 3 is modified such that the output of the capacitance-to-voltage converting unit 1 is connected to the non-inverting input terminal of the operational amplifier AMP3 through a resistor R6', and an AC bias voltage Vs is applied to the inverting input terminal of the operational amplifier AMP3 through a resistor R7'.

In the following, the operation of the static capacitance-to-voltage converter of Fig. 8 will be described from a mathematical viewpoint. In Fig. 8, the following equations are satisfied:

$$Va = Vin[1+R1 \cdot j\omega(Cx+Cp)$$

$$Vb = Vin$$

$$Vc = (R7/R6)Vin+[1+(R7/R6)] \times [R7'/(R6'+R7')]Va$$

$$Vd = [(1+R4/R3)/(1+R5 \cdot j\omega C1) - R4/R3]Vb$$

$$Ve = (R11/R10)Vd$$

$$Vout = -(R9/R8)Vc+[1+(R9/R8)] \times [R13/(R12+R13)]Ve$$

Therefore, the output voltage Vout of the adder 6 is expressed by the following equation:

$$Vout = (R9/R8)(R7/R6)Vin-\{[1+R7/R6)] \times [R7'/(R6'+R7')][1+R1 \cdot j\omega(Cx+Cp)]\}Vin-\{[1+(R9/R8)] \times [R15/(R12/R3)](R11/R10) \times [1+(R4/R3)]/(1+R5 \cdot j\omega C1) - (R4/R3)\}Vin$$

Here, when the resistances are selected such that R3=R4, R6=R7, R6'=R7', R8=R9, R10=R11, and R12=R13 are satisfied, the output voltage Vout of the adder 6 can be rewritten as follows:

$$Vout = \{[R5 \cdot j\omega C1-1)/(1+R5 \cdot j\omega C1)] - R1 \cdot j\omega(Cx+Cp)\}Vin \quad (10)$$

When the static capacitance element 14 is not connected to the signal line 13, i.e., when Cx=0, the amplitude of the output voltage of the capacitance-to-voltage converting unit 1 and the angular frequency, amplitude and phase of the AC signal output from the AC signal generator 4 are adjusted such that Vout in the equation (10) is zero. Substituting 0 into Vout (Vout=0) and 0 into Cx (Cx=0) in the equation (10) for finding a condition in which Vout is zero, the equation (10) can be

rewritten as follows:

$$[(R5 \cdot j\omega C1-1)/(1+R5 \cdot j\omega C1)]-R1 \cdot j\omega Cp = 0 \quad (11)$$

From this equation,

$$R5C1 = R1Cp \quad (12)$$

$$\omega = 1/(R5C1R1Cp)^{1/2} \quad (13)$$

are derived. Thus, Vout can be made zero by adjusting R5, C1 and ω, so as to satisfy the equations (12) and (13) in a state in which the static capacitance element 14 is not connected to the signal line 13.

Next, when the static capacitance element 14 is connected to the signal line 13, the equation (10) can be rewritten as follows since the equations (11), (12) and (13) are satisfied as mentioned above:

$$Vout = VinR1 \cdot j\omega Cx \quad (14)$$

This equation (14) indicates that the output voltage Vout of the adder 6 is not influenced at all by any static capacitance other than the static capacitance Cx of the static capacitance element 14.

As described above in detail, since the static capacitance-to-voltage converter according to the second embodiment illustrated in Figs. 7 and 8 also cancels a stray capacitance formed between the signal line 13 and the shielding line 15, and a stray capacitance formed between the exposed portion of the signal line 13 and its surroundings, it can output a voltage exactly corresponding to the static capacitance Cx of the static capacitance element 14 without suffering from the influence of such stray capacitances.

In the description heretofore made in connection with the static capacitance-to-voltage converter of Fig. 8, connecting the static capacitance element 14 having the static capacitance Cx to the signal line 13 is equivalent to a change in the static capacitance connected to the inverting input terminal of the operational amplifier AMP1 by Cx. Therefore, the static capacitance-to-voltage converter of Fig. 8 can also output a voltage exactly corresponding to ΔCx when the static capacitance Cx of the static capacitance element 14 connected to the signal line 13 has changed by ΔCx. In the following, this operation will be described in detail.

The output voltage Vout of the adder 6 when the static capacitance element 14 is connected to the signal line 13 is expressed by the aforementioned equation (10). Assume that Vout is zero in this state. Conditions for satisfying this can be found by substituting 0 into Vout (Vout=0) in the equation (10):

$$R5C1 = R1(Cx+Cp) \quad (15)$$

$$\omega = 1/[R5C1R1(Cx+Cp)^{1/2}$$

$$= 1/R5C1 \quad (16)$$

Stated another way, the output voltage Vout of the adder 6 can be made zero by adjusting the angular frequency ω of the AC signal from the AC signal generator 4, R5 and C1 to satisfy the equations (15) and (16).

Next, the output voltage Vout of the adder 6, when the static capacitance Cx of the static capacitance element 14 has changed by ΔCx, can be expressed by substituting $Cx+\Delta Cx$

for Cx in the equation (10):

$$Vout = \{[R5 \cdot j\omega C1-1)/(1+R5 \cdot j\omega C1)] -R1 \cdot j\omega(Cx+\Delta Cx+Cp)\}Vin \quad (17)$$

Then, substituting the equations (15) and (16) into the equation (17), and giving Vout=0 in the equation (17):

$$Vout = -VinR1 \cdot j\omega\Delta Cx \quad (18)$$

This equation indicates that Vout exactly corresponds to ΔCx. This equation also indicates that the static capacitance-to-voltage converter of Fig. 8 is capable of outputting a voltage exactly corresponding to a change in capacitance of the static capacitance element 14 connected to the signal line 13.

While the foregoing description has also been made on the assumption that Vs=0 is satisfied, the same conclusion is derived except that associated calculations are more complicated. Alternatively, in Figs. 7 and 8, a subtractor may be used in place of the adder 6 such that the subtractor is applied with the output of the first amplitude adjuster 3 and the output of the second amplitude adjuster 5 which are adjusted to have the same amplitude and the same phase.

Fig. 9 illustrates the configuration of a capacitance meter which applies the static capacitance-to-voltage converter illustrated in Fig. 7. This capacitance meter, similar to the capacitance meter illustrated in Fig. 5, has an integrator 16 connected to the adder 6, and outputs of the integrator 16 and the AC signal generator 4 connected to a phase comparator 17. While in the layout illustrated in

Figs. 3 and 4, high harmonic components of the AC signal Vin output from the AC signal generator 4 may be introduced into the phase adjuster 2 or the first amplitude adjuster 3, the introduction of such high harmonic components can be effectively prevented by disposing the phase adjuster 2 at a position illustrated in Fig. 9.

As stated above, the output voltage Vout of the adder 6 is expressed by the equations (14) and (18). By integrating this voltage by the integrator 16, it is possible to produce a voltage E which is proportional to the static capacitance Cx of the static capacitance element 14 or a change ΔCx in the static capacitance Cx. Also, by using the phase comparator 17 to derive a difference in phase between the voltage E output from the integrator 16 and the AC signal Vin output from the AC signal generator 4, dielectric loss tangent can be derived for the static capacitance element 14.

In a manner similar to the capacitance meter of Fig. 5, the capacitance meter of Fig. 9 may also be designed such that one electrode 14_1 of the static capacitance element 14 is used as a measuring electrode, and the other electrode 14_2 is used as an object under measurement for which a determination is made as to whether it is good or bad based on the magnitude of a static capacitance Cx formed between the one electrode 14_1 and the other electrode 14_2. In this case, a housing for the capacitance meter is provided with a case having the same electric potential (voltage) as the operational amplifier 11. After the measuring electrode is

accommodated in this case, the output voltage Vout of the adder 6 is adjusted to minimum or zero. In this event, if the measuring electrode is taken out of the case during a measurement, the adder 6 experiences a drift by a voltage proportional to a stray capacitance between the measuring electrode and its surroundings. Therefore, a static capacitance between the measuring electrode and the object under measurement can be more accurately measured by correcting the phase adjuster 2, the first amplitude adjuster 3 and the second amplitude adjuster 5 such that the drift value becomes minimum or zero. It is revealed from the foregoing that the capacitor meter of Fig. 9 is capable of measuring a very small static capacitance, as is the case of the capacitance meter of Fig. 5.

Fig. 10 is a block diagram generally illustrating an exemplary modification to the capacitor meter illustrated in Fig. 9, where the output of the integrator 16 in Fig. 9 is connected to a first synchronous detector 18 and a second synchronous detector 19, such that these synchronous detectors 18, 19 are applied with an AC signal Vin from an AC signal generator 4. When the first synchronous detector 18 synchronously detects a voltage E output from the integrator 16 with the AC signal Vin which is in phase with the voltage E, the static capacitance Cx of a static capacitance element 14 or a change ΔCx in the static capacitance Cx can be derived as an output of the first synchronous detector 18. Similarly, when the second synchronous detector 19 synchronously detects the voltage E

from the integrator 16 with the AC signal Vin which is out of phase by 90° from the voltage E, dielectric loss tangent for the static capacitance element 14 can be derived as an output of the second synchronous detector 19.

More specifically, the static capacitance Cx of the static capacitance element 14 can be derived by the first synchronous detector 18 as an average value or an integrated value of the voltage E over a range from 0° to 180° with respect to the phase of the AC signal Vin from the AC signal generator 4. Also, the dielectric loss tangent for the static capacitance Cx of the static capacitance element 14 can be derived by the second synchronous detector 19 as an average value or an integrated value of the voltage E over a range from 90° to 270° with respect to the phase of the AC signal Vin from the AC signal generator 14.

In the two embodiments described above, an example of the static capacitance element 14 having a static capacitance to be converted into a voltage may be a capacitive sensor which has one electrode connected to the inverting input terminal (-) of the operational amplifier AMP1 of the capacitance-to-voltage converting unit 1 through the signal line 13, and the other electrode (or a counterpart corresponding thereto) grounded, clamped at an appropriate bias electric potential (voltage), or opened in a space without being grounded. Such capacitive sensors may include all devices for detecting a static capacitance as well as known capacitive sensor such as an acceleration sensor, seismometer, pressure sensor, displacement sensor,

displacement meter, proximity sensor, touch sensor, ion sensor, humidity sensor, rain drop sensor, snow sensor, lightening sensor, alignment sensor, touch failure sensor, shape sensor, end point detecting sensor, vibration sensor, ultrasonic sensor, angular velocity sensor, liquid amount sensor, gas sensor, infrared sensor, radiation sensor, level meter, freezing sensor, moisture meter, vibration meter, charge sensor and printed board tester. In addition, the present invention may also be applied to a clamp-type voltage meter or the like which measures a voltage in a contactless form.

Also, in the first and second embodiments, one electrode 14_1 of the static capacitance element 14 may be used as a measuring electrode, while the other electrode 14_2 is used as an object under measurement for which a determination is made as to whether it is good or bad based on the magnitude of a static capacitance Cx formed between the one electrode 14_1 and the other electrode 14_2.

For the purpose of verifying the operation of the static capacitance-to-voltage converter, the static capacitance-to-voltage converter structured such as shown in Fig. 4 was formed to obtain a relation between the output voltage Vout (mV) and the static capacitance Cx (fF). As a result, a linear relation between Cx and Vout was obtained, and it was made sure that we could measure no more than 1 - 3 femtofarad, as shown in Fig. 4.

INDUSTRIAL APPLICABILITY

As will be apparent from the foregoing description

with reference to the illustrated embodiments, the present invention produces the following effects:

(1) The static capacitance of a static capacitance element connected to a signal line can be converted into a voltage without suffering from the influence of a stray capacitance formed between the signal line and a shielding line surrounding the signal line or a stray capacitance formed between an exposed portion of the signal line and its surroundings to derive a voltage exactly corresponding to the static capacitance, thereby making it possible to make highly accurate conversion of the static capacitance of a static capacitance element into a voltage and detect the voltage even if the static capacitance is very small, for example, on the order of femtofarad (1/1000 of picofarad).

(2) Even if an electrode of a static capacitance element, which is not connected to a signal line, is biased at a certain electric potential (voltage), it is possible to produce a voltage exactly corresponding to the static capacitance of the static capacitance element.

(3) Since the static capacitance of a static capacitance element can be converted into a signal which includes the static capacitance and the frequency of an AC signal, the conversion of the static capacitance into a voltage and detection of the voltage can be achieved even if the AC signal has a low frequency under about 10 MHz..

CLAIMS

1. A static capacitance-to-voltage converter comprising:

an operational amplifier having an inverting input terminal, a non-inverting input terminal and an output terminal, said operational amplifier having said output terminal and said inverting input terminal connected through a feedback resistor;

a signal line having one end connected to said inverting input terminal and the other end capable of being connected to a static capacitance element having a static capacitance;

a shield surrounding at least a portion of said signal line, and connected to said non-inverting input terminal;

alternate current signal generator for applying said non-inverting input terminal with an alternate current signal; and

an adjuster connected to the output terminal of said operational amplifier and an output terminal of said alternate current signal generator for adjusting an output of said static capacitance-to-voltage converter to minimum when no static capacitance element is connected to said signal line.

2. A static capacitance-to-voltage converter comprising:

an operational amplifier having an inverting input terminal, a non-inverting input terminal and an output terminal, said operational amplifier having said output terminal and said inverting input terminal connected through a feedback resistor;

a signal line having one end connected to said inverting input terminal and the other end capable of being connected to a static capacitance element having a static capacitance;

a shield surrounding at least a portion of said signal line, and connected to said non-inverting input terminal;

alternate current signal generator for applying said non-inverting input terminal with an alternate current signal;

a variable the frequency generator of said alternate current signal; and

an adjusting circuit for adjusting amplitudes and phases of an output signal of said operational amplifier and said alternate current signal such that they are canceled with each other.

3. A static capacitance-to-voltage converter according to claim 2, wherein said adjusting circuit comprises:

first adjuster for adjusting the amplitude of said alternate current signal;

second adjuster for adjusting the phase and amplitude of an output voltage from said operational amplifier such said output voltage has the same amplitude as and an opposite phase to an output of said first adjuster; and

an adder for adding the output of said first adjuster and an output of said second adjuster.

4. A static capacitance-to-voltage converter according to claim 2, wherein said adjusting circuit comprises:

third adjuster for adjusting the amplitude of the

output voltage of said operational amplifier;

fourth adjuster for adjusting the phase and amplitude of said alternate current signal such that said alternate current signal has the same amplitude as and an opposite phase to an output of said third adjuster; and

an adder for adding the output of said third adjuster and an output of said fourth adjuster.

5. A static capacitance-to-voltage converter according to any of claims 1 - 4, further comprising integrator for integrating an output of said adjuster, wherein when a static capacitance is connected to the other end of said signal line, a signal corresponding to the static capacitance of said static capacitance is produced as an output of said integrator.

6. A static capacitance-to-voltage converter according to claim 5, further comprising comparator for comparing the phase of the output of said integrator with the phase of said alternate current signal, wherein when a static capacitance is connected to the other end of said signal line, a signal representative of dielectric loss tangent for the static capacitance of said static capacitance element is produced as an output of said comparator.

7. A static capacitance-to-voltage converter according to claim 5, further comprising first and second synchronous detectors for receiving the output of said integrator and said alternate current signal, said first synchronous detector outputting a signal representative of the static capacitance of said static capacitance, and said second

synchronous detector outputting a signal representative of dielectric loss tangent for the static capacitance of said static capacitance.

8. A static capacitance-to-voltage converter according to any of claims 1 - 7, wherein said shield surrounds said signal line over the entire length thereof.

9. A static capacitance-to-voltage converter according to any of claims 1 - 8, wherein said static capacitance is a capacitive sensor.

10. A static capacitance-to-voltage converter according to any of claims 1 - 9, wherein said static capacitance comprises a measuring electrode connected to the other end of said signal line so that a static capacitance is formed between an object under measurement and said measuring electrode.

11. A static capacitance-to-voltage converter according to claim 10, further comprising a case placed at the same voltage as the non-inverting input terminal of said operational amplifier, for accommodating said measuring electrode when no static capacitance is connected to said signal line, wherein said adjuster adjusts the output of said static capacitance-to-voltage converter to minimum when said measuring electrode is accommodated in said case.

12. A method of converting a static capacitance into a voltage comprising:

connecting one end of a signal line to said inverting input terminal, said signal line having at least a portion thereof surrounded by a shield;

placing said shield at the same potential as said non-inverting input terminal;

applying an alternate current signal to said non-inverting input terminal;

adjusting an output signal of said operational amplifier and said alternate current signal such that said output signal and said alternate current signal are canceled with each other when no static capacitance is connected to the other end of said signal line; and

connecting a static capacitance to the other end of said signal line, after said adjusting, to retrieve a voltage signal corresponding to the static capacitance of said static capacitance.

13. A method of converting a static capacitance into a voltage according to claim 12, wherein said adjusting an output signal of said operational amplifier and said alternate current signal such that said output signal and said alternate current signal are canceled with each other when no static capacitance is connected to the other end of said signal line comprises:

varying the frequency of said alternate current signal; and

adjusting the output signal of said operational amplifier and said alternate current signal in phase and amplitude such that said output signal and said alternate current signal are canceled with each other.

14. A method of converting a static capacitance into a voltage according to claim 13, wherein said adjusting an

output signal of said operational amplifier and said alternate current signal such that said output signal and said alternate current signal are canceled with each other when no static capacitance is connected to the other end of said signal line comprises:

adjusting the amplitude of said alternate current signal;

adjusting the phase and amplitude of an output voltage from said operational amplifier such said output voltage has the same amplitude as and an opposite phase to said alternate current signal having its amplitude adjusted; and

adding said alternate current signal having its amplitude adjusted, and the output voltage of said operational amplifier having its phase and amplitude adjusted.

15. A method of converting a static capacitance into a voltage according to claim 13, wherein said adjusting an output signal of said operational amplifier and said alternate current signal such that said output signal and said alternate current signal are canceled with each other when no static capacitance is connected to the other end of said signal line comprises:

adjusting the amplitude of an output voltage of said operational amplifier;

adjusting the phase and amplitude of said alternate current signal such that said alternate current signal has the same amplitude as and an opposite phase to the output voltage of said operational amplifier having its amplitude

adjusted; and

adding said output voltage having its amplitude adjusted and said alternate current signal having its phase and amplitude adjusted.

16. A method of converting a static capacitance into a voltage according to any of claims 12 - 15, further comprises integrating said voltage signal to output a signal corresponding to said static capacitance.

17. A method of converting a static capacitance into a voltage according to claim 16, further comprises comparing the phase of said integrated signal with the phase of said alternate current signal to output a signal representative of dielectric loss tangent for said static capacitance.

18. A method of converting a static capacitance into a voltage according to claim 16, further comprising synchronously detecting said integrated signal with said alternate current signal to output a signal representative of the static capacitance and a signal representative of dielectric loss tangent for the static capacitance.

19. A method of converting a static capacitance into a voltage according to any of claims 12 - 18, wherein said shield is a shielding line surrounding said signal line over its entire length.

20. A method of converting a static capacitance into a voltage according to any of claims 12 - 19, wherein said static capacitance is a capacitive sensor.

21. A method of converting a static capacitance into a voltage according to any of claims 12 - 20, wherein said

static capacitance comprises a measuring electrode so that a static capacitance is formed between an object under measurement and said measuring electrode.

22. A method of converting a static capacitance into a voltage according to claim 21, further comprising:

accommodating said measuring electrode in a case during measurement waiting time, said case being placed at the same voltage as a non-inverting input terminal of said operational amplifier; and

performing a zero adjustment to cancel a stray capacitance formed between said measuring electrode and its ambient.

Fig. 1 (PRIOR ART)

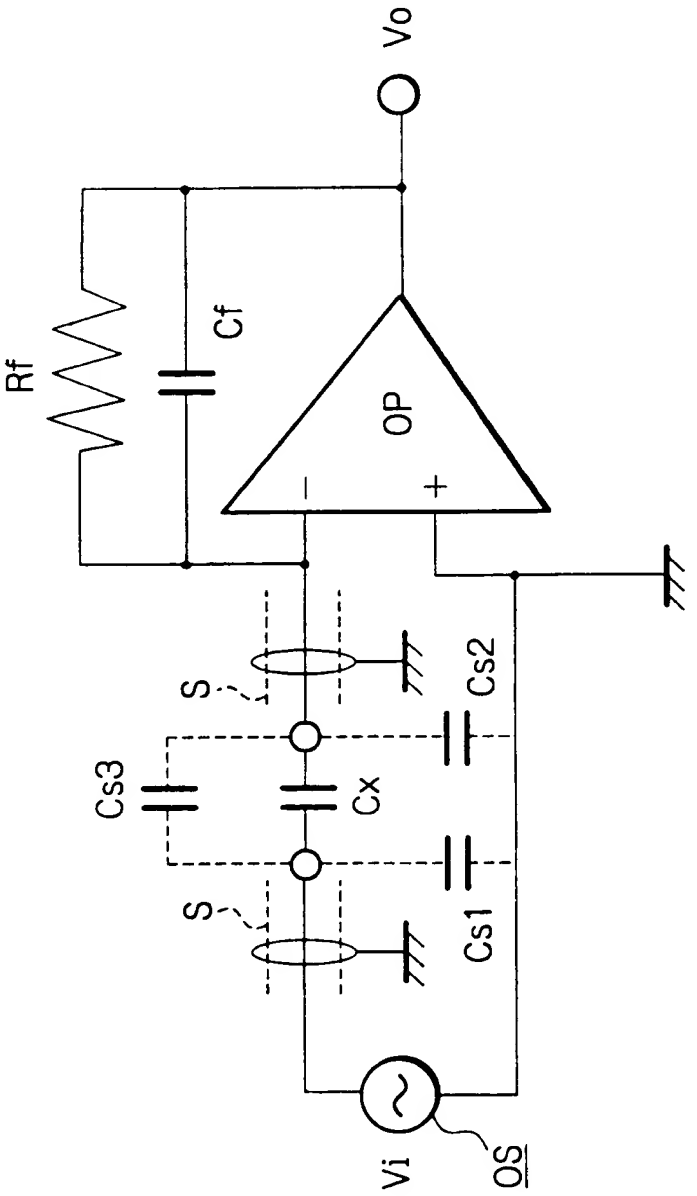


Fig. 2

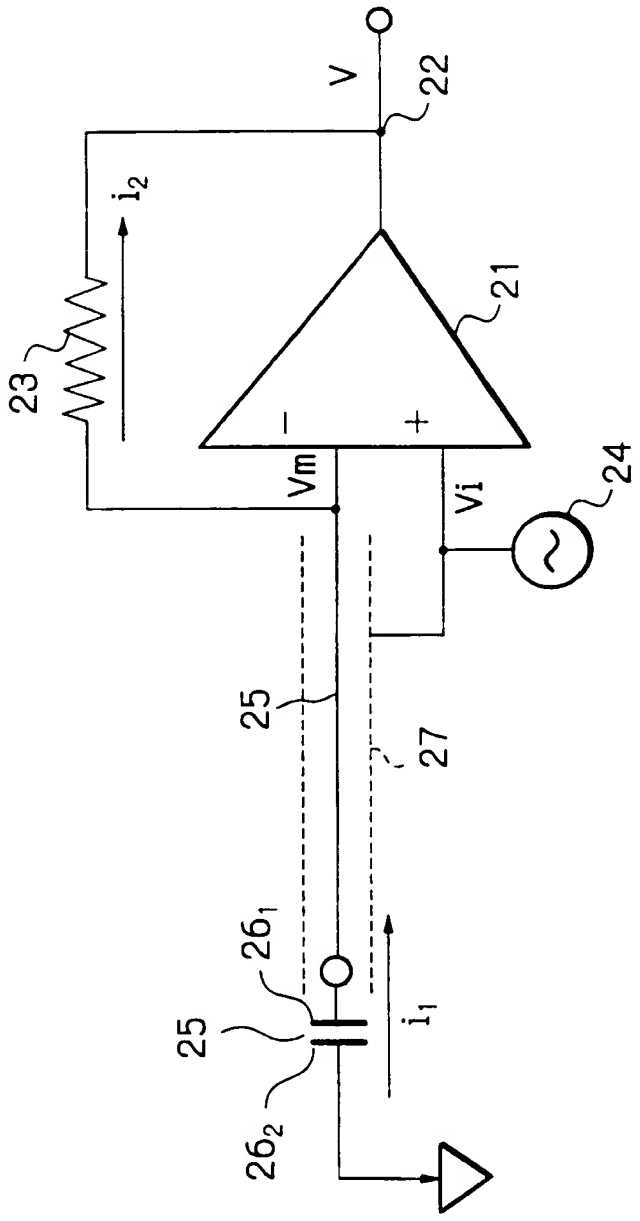


Fig. 3

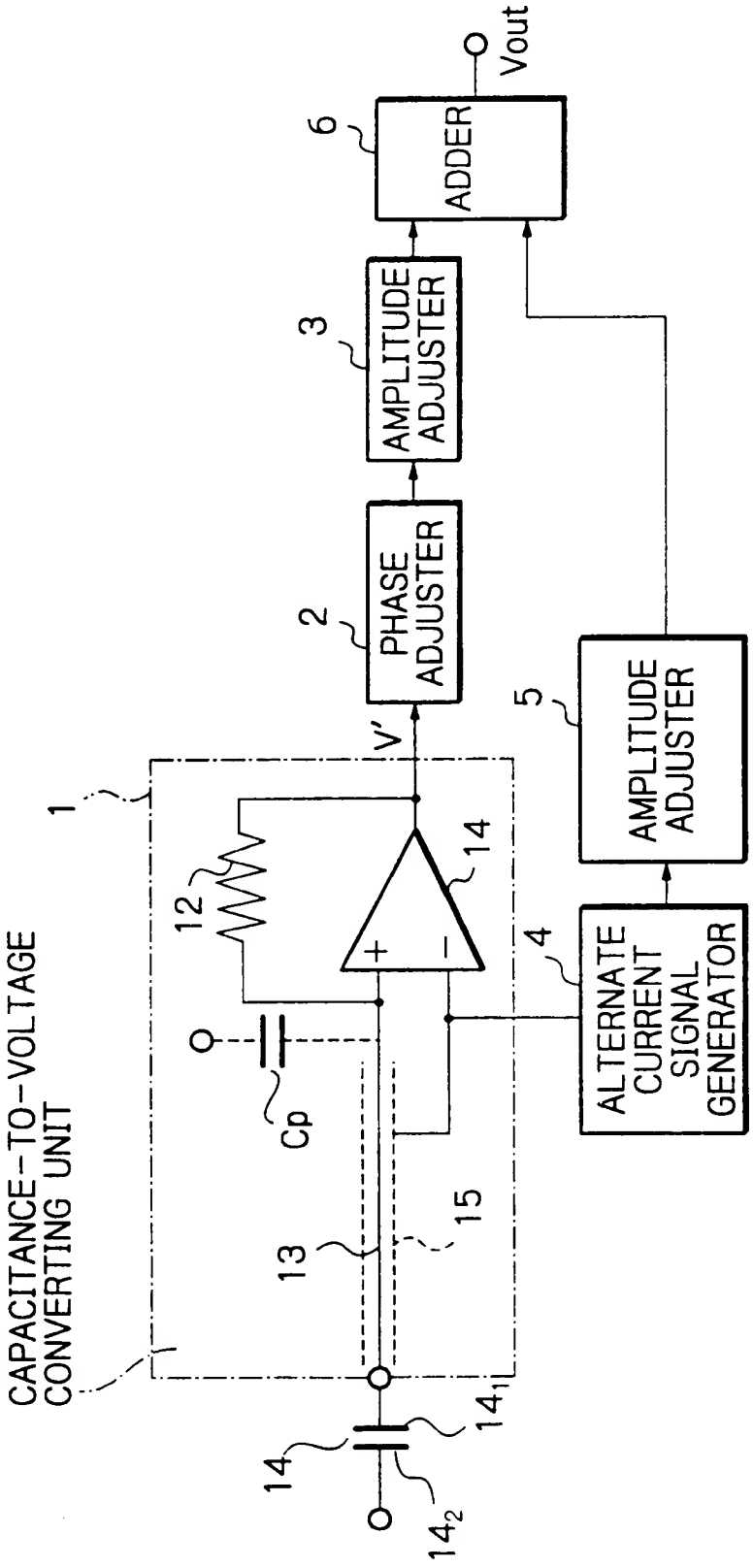

CAPACITANCE-TO-VOLTAGE CONVERTING UNIT
1
12
14
+
−
V'
2
PHASE ADJUSTER
3
AMPLITUDE ADJUSTER
6
ADDER
Vout
5
AMPLITUDE ADJUSTER
4
ALTERNATE CURRENT SIGNAL GENERATOR
Cp
13
15
14
14₁
14₂

Fig. 4

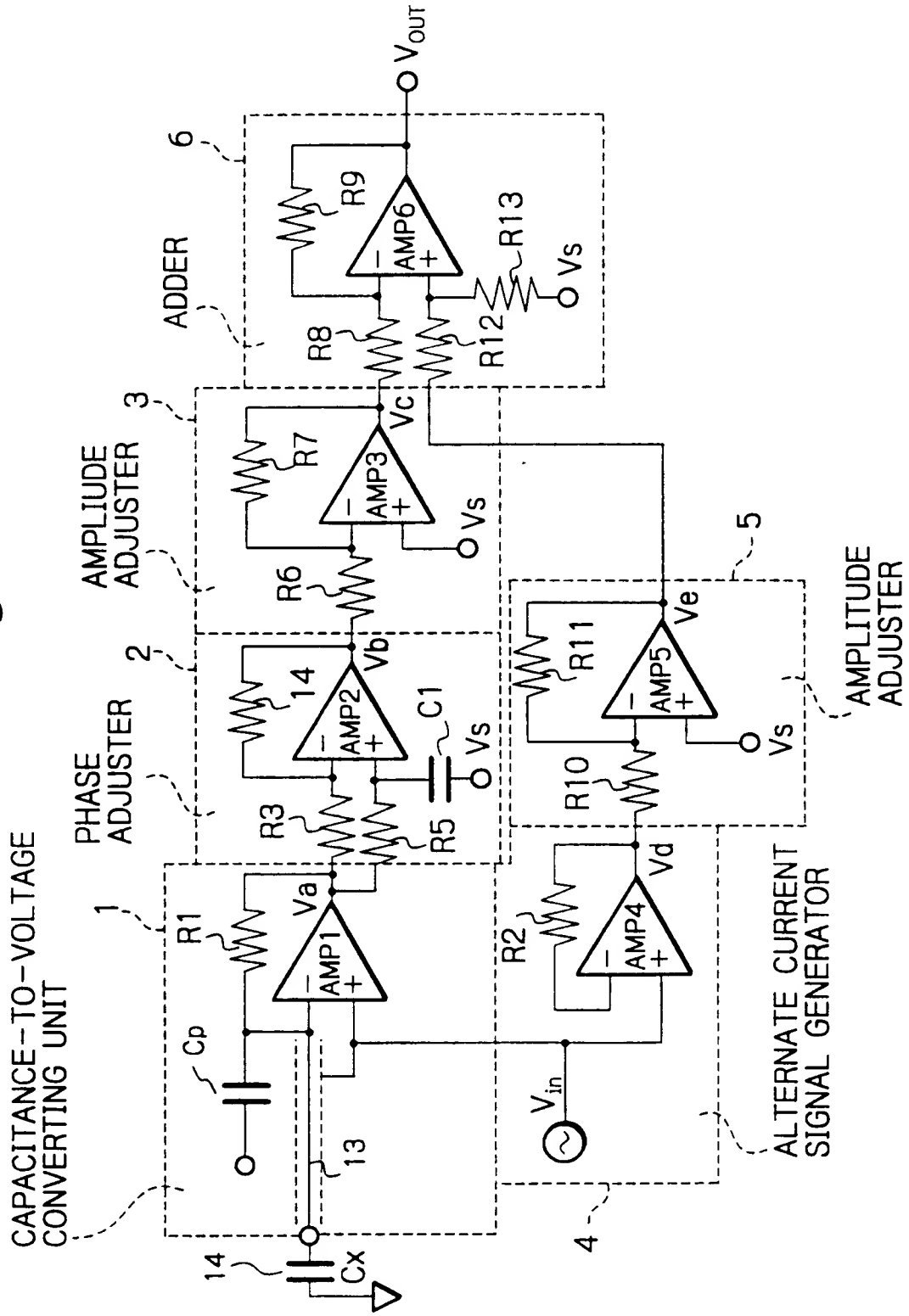
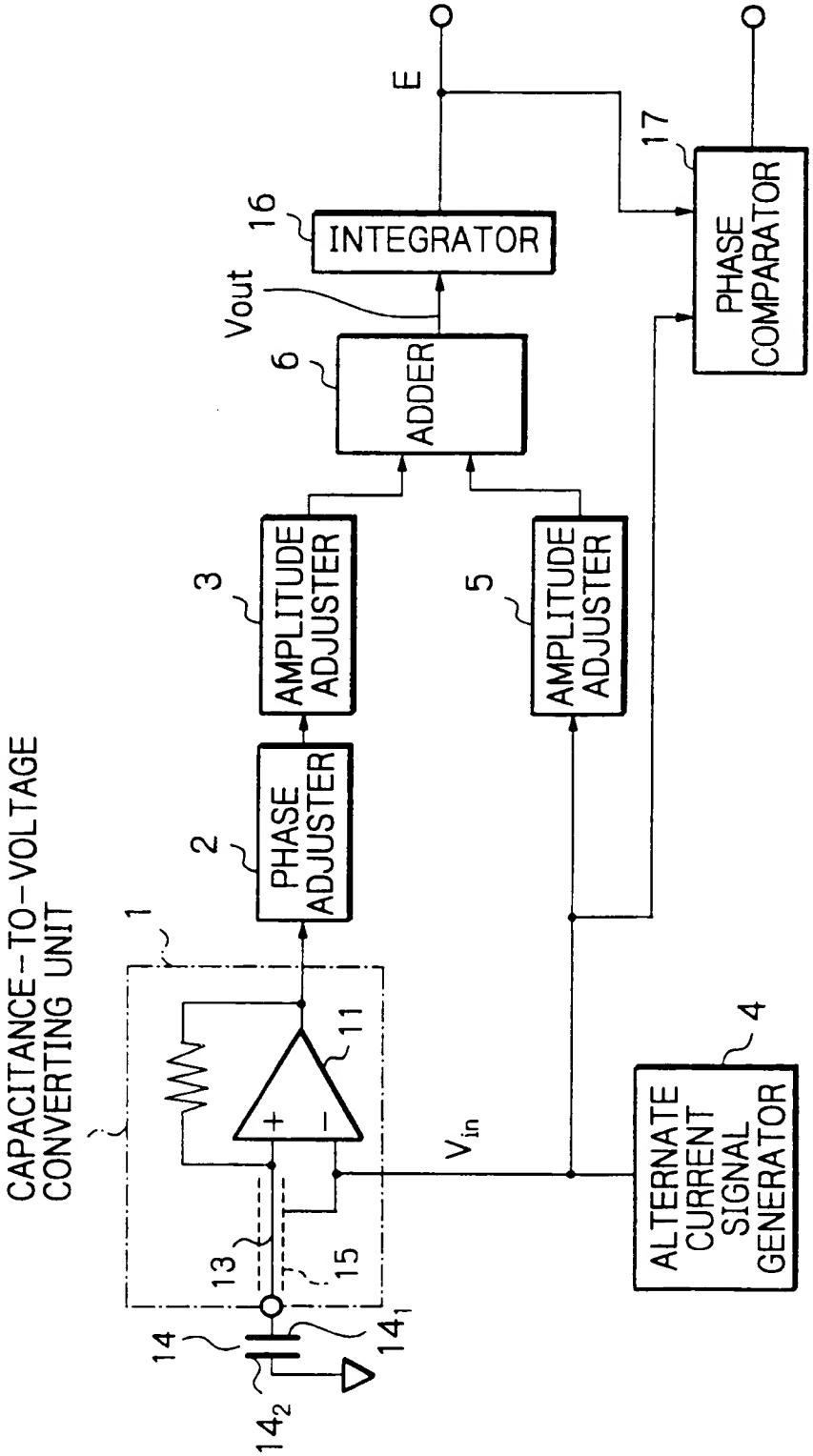

CAPACITANCE-TO-VOLTAGE CONVERTING UNIT
PHASE ADJUSTER
AMPLIUDE ADJUSTER
ADDER
AMPLITUDE ADJUSTER
ALTERNATE CURRENT SIGNAL GENERATOR
1
2
3
4
5
6
AMP1
AMP2
AMP3
AMP4
AMP5
AMP6
R1
R2
R3
R5
R6
R7
R8
R9
R10
R11
R12
R13
14
C1
Cp
Cx
13
Va
Vb
Vc
Vd
Ve
Vs
V_{OUT}
V_{in}

Fig. 5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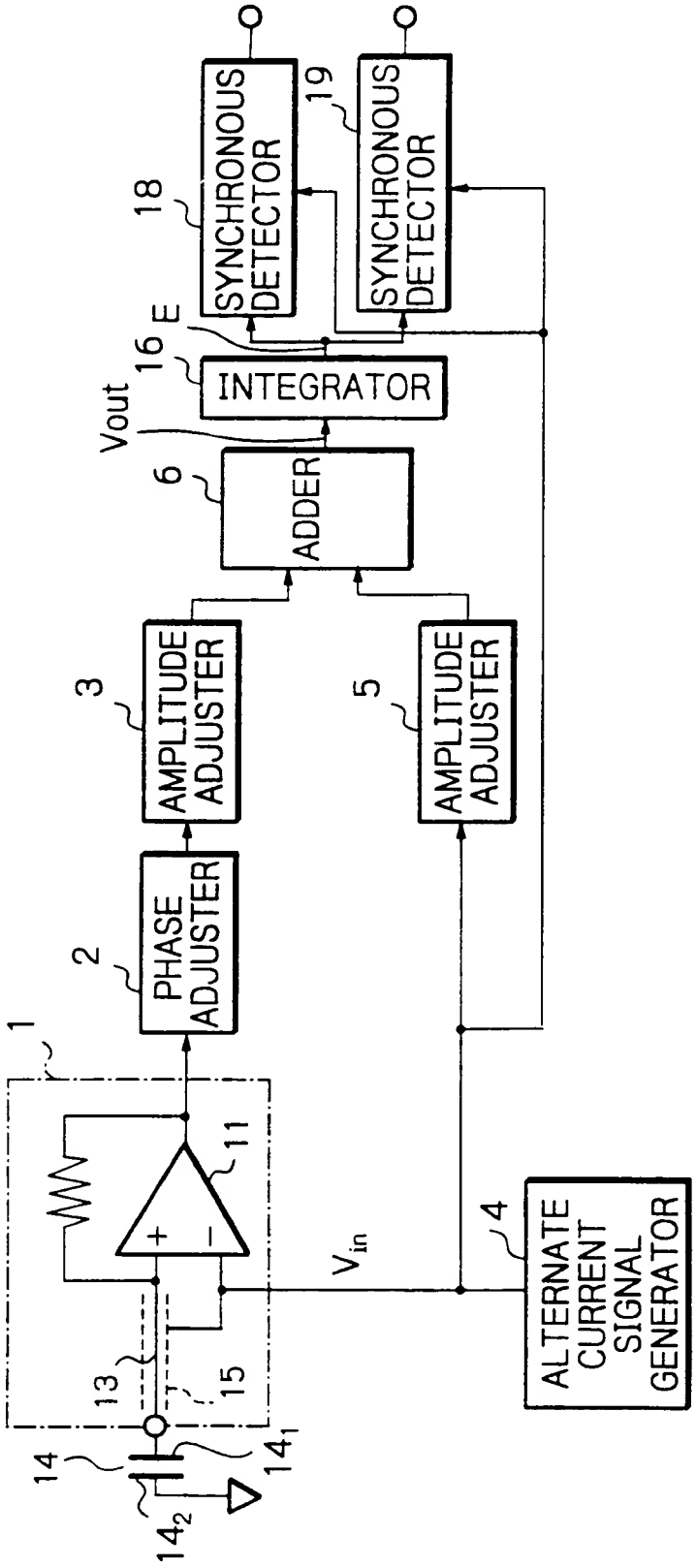
2
PHASE ADJUSTER
3
AMPLITUDE ADJUSTER
5
AMPLITUDE ADJUSTER
6
ADDER
16
INTEGRATOR
17
PHASE COMPARATOR
4
ALTERNATE CURRENT SIGNAL GENERATOR
11
13
15
14
14₁
14₂
Vout
E
Vin

Fig. 6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SYNCHRONOUS DETECTOR
19
E
16
INTEGRATOR
Vout
6
ADDER
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AMPLITUDE ADJUSTER
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AMPLITUDE ADJUSTER
2
PHASE ADJUSTER
1
11
13
15
14
14₁
14₂
Vin
4
ALTERNATE CURRENT SIGNAL GENERATOR

Fig. 7

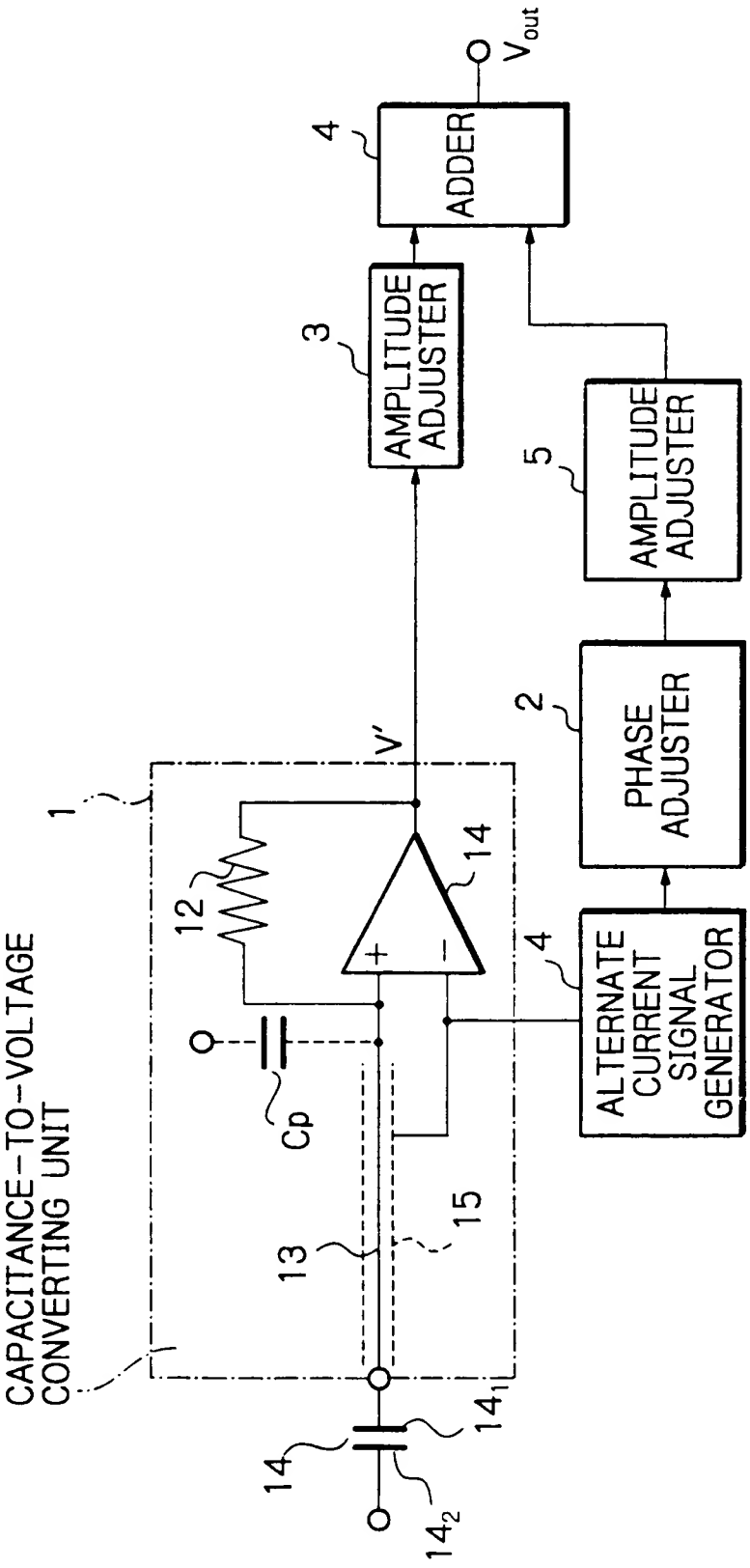

V_{out}
ADDER
4
AMPLITUDE ADJUSTER
3
AMPLITUDE ADJUSTER
5
PHASE ADJUSTER
2
ALTERNATE CURRENT SIGNAL GENERATOR
4
V'
1
12
14
+
-
Cp
13
15
CAPACITANCE-TO-VOLTAGE CONVERTING UNIT
14_1
14
14_2

Fig. 8

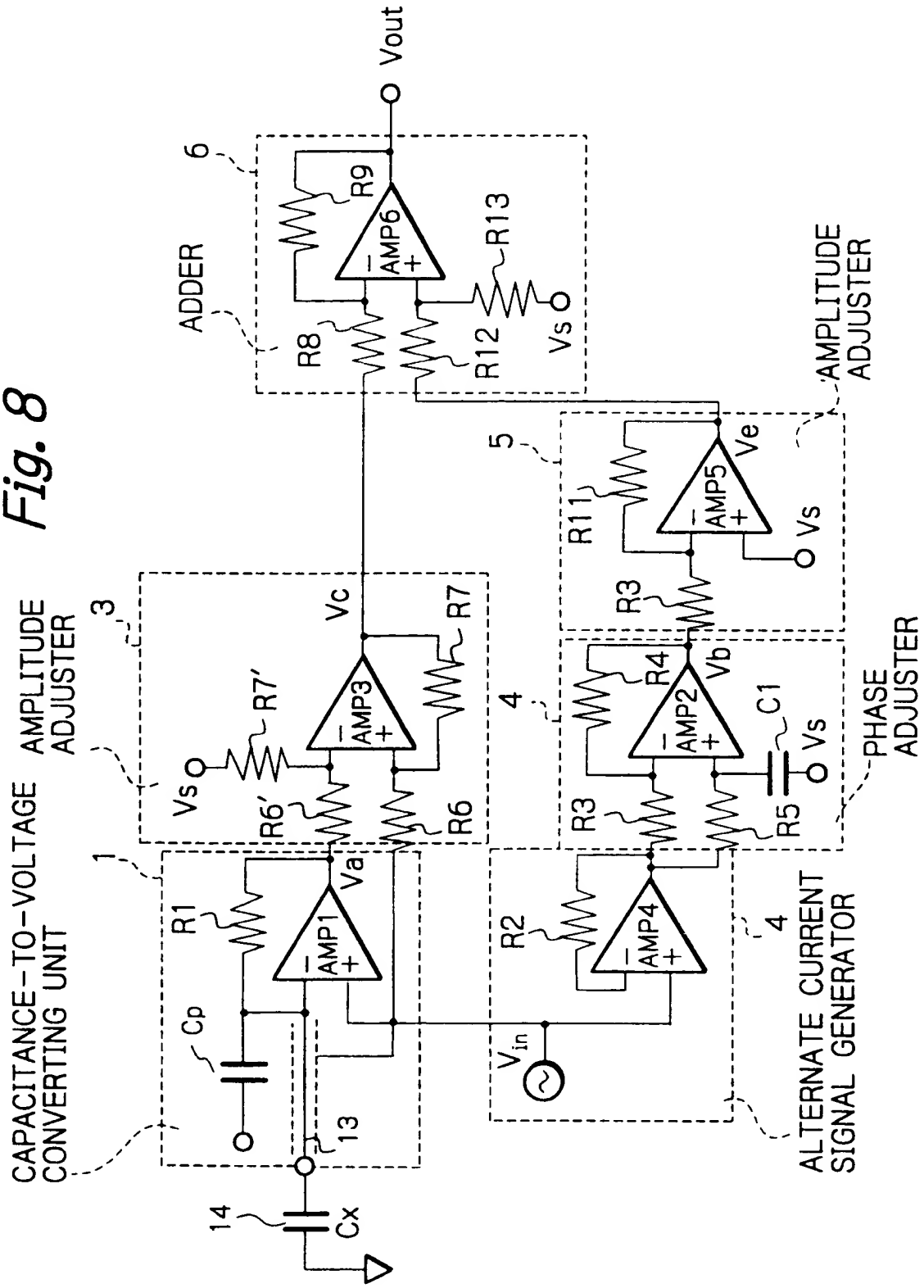
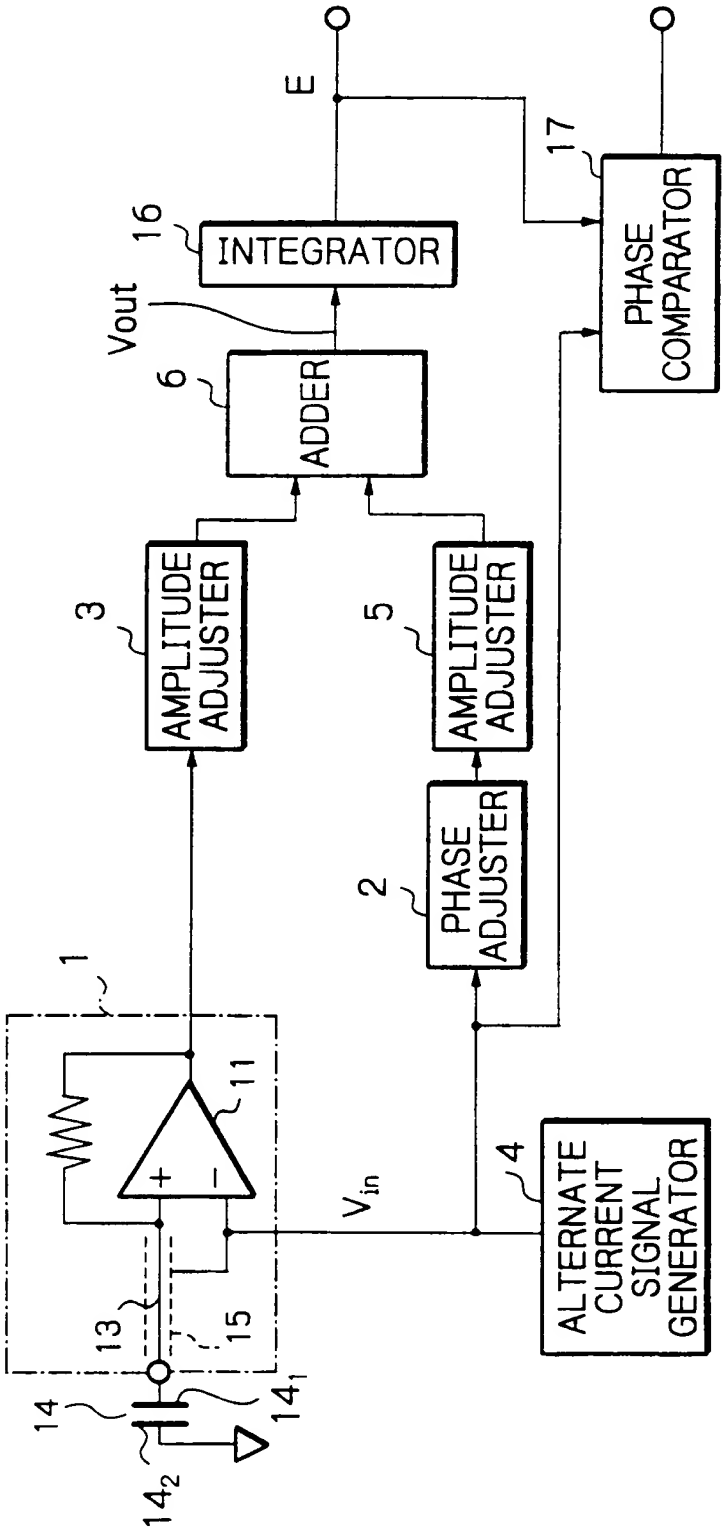

Vout
6
ADDER
R9
AMP6
R13
R8
R12
Vs
AMPLITUDE ADJUSTER
5
R11
AMP5
Ve
Vs
R3
3
AMPLITUDE ADJUSTER
Vc
R7
R7'
AMP3
Vs
R6'
R6
4
R4
Vb
AMP2
C1
Vs
R3
R5
PHASE ADJUSTER
1
CAPACITANCE-TO-VOLTAGE CONVERTING UNIT
R1
Va
AMP1
Cp
13
14
Cx
R2
AMP4
V_{in}
4
ALTERNATE CURRENT SIGNAL GENERATOR

Fig. 9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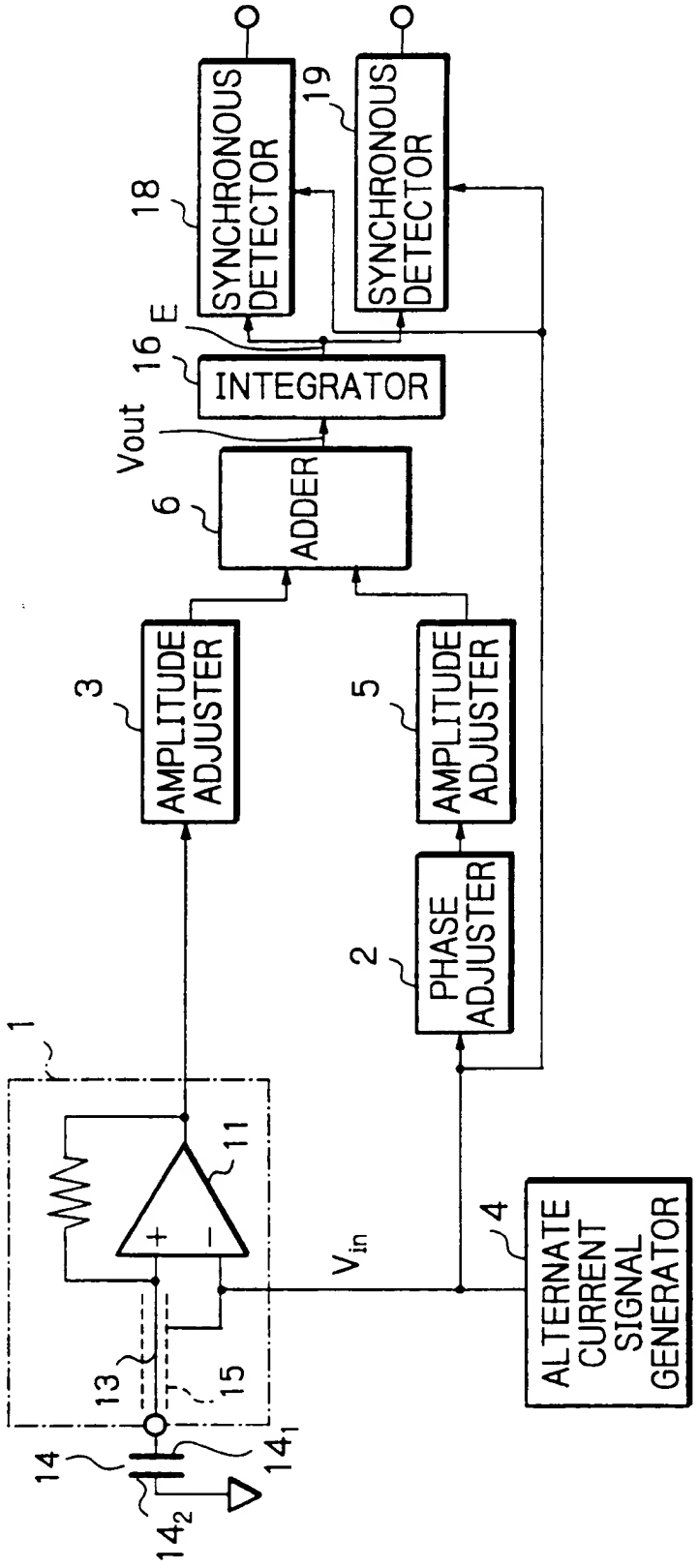
17
16
INTEGRATOR
Vout
6
ADDER
PHASE COMPARATOR
3
AMPLITUDE ADJUSTER
5
AMPLITUDE ADJUSTER
2
PHASE ADJUSTER
1
11
+
−
V_{in}
4
ALTERNATE CURRENT SIGNAL GENERATOR
13
15
14
14_1
14_2

Fig. 10


SYNCHRONOUS DETECTOR
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SYNCHRONOUS DETECTOR
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INTEGRATOR
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Vout
ADDER
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AMPLITUDE ADJUSTER
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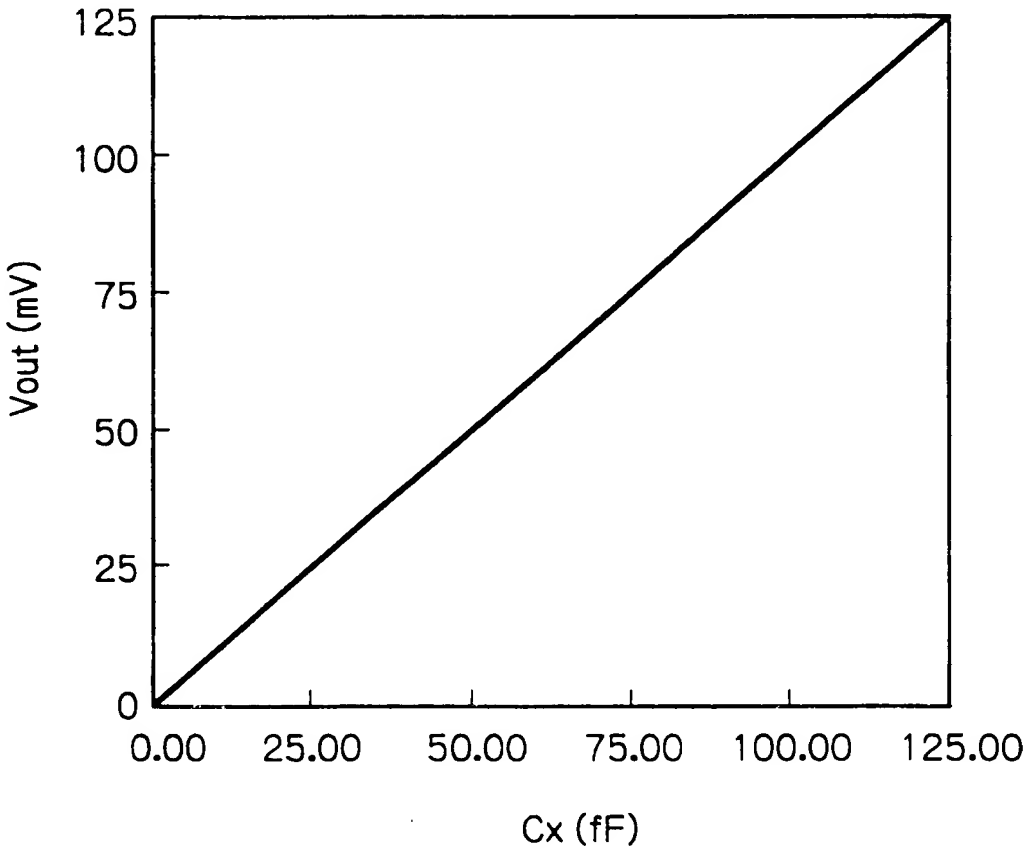
AMPLITUDE ADJUSTER
5
PHASE ADJUSTER
2
1
11
V_{in}
4
ALTERNATE CURRENT SIGNAL GENERATOR
13
15
14
14_1
14_2

Fig. 11



INTERNATIONAL SEARCH REPORT

Inte. ɔnal Application No
PCT/JP 99/00229

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R27/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	PATENT ABSTRACTS OF JAPAN vol. 98, no. 2, 30 January 1998 & JP 09 280806 A (NISSAN MOTOR), 31 October 1997	1
A	see abstract	2,9,10, 12,20,21

Y	GB 2 020 816 A (MICRO-SENSORS INC.) 21 November 1979	1
A	see page 2, line 103 - line 111 see page 3, line 42 - line 65; figure 2	2,12

A	US 4 918 376 A (PODUJE ET AL.) 17 April 1990	1,2,12
	see column 3, line 1 - line 17; figure 1	

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 April 1999	03/05/1999

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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/JP 99/00229

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No
A	MONTICELLI ET AL.: "OP-AMP CIRCUIT MEASURES DIODE-JUNCTION CAPACITANCE" ELECTRONICS. DE 1984 A 1985 : ELECTRONICS WEEK., vol. 48, no. 14, 10 July 1975, pages 112-113, XP002100006 NEW YORK US see the whole document	

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter ...nal Application No
PCT/JP 99/00229

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2020816 A	21-11-1979	NONE	
US 4918376 A	17-04-1990	JP 2068749 C	10-07-1996
		JP 7094964 B	11-10-1995